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IN THE CLAIMS

Claims 1-20 (Canceled)

21. (Currently Amended) A disk drive for reading information from a disk and outputting the read information which is to be provided to a host, comprising:

an accessing circuit which accesses the disk and generates the read information from the disk;

an interface circuit which transfers the generated read information from the accessing circuit to the host; and

a microcomputer, coupled with the accessing circuit and with the interface circuit, being located on a semiconductor substrate and including a central processing unit and an electrically erasable and programmable nonvolatile memory,

wherein the electrically erasable and programmable nonvolatile memory stores a first program, a second program and a third program,

wherein using the stored first program, the microcomputer controls the accessing circuit so that the operation of the accessing circuit is controlled by the stored first program,

wherein using the stored second program, the microcomputer is adapted to check data in the electrically erasable and programmable nonvolatile memory, and

wherein using the stored third program, in response to the result of the check by using the stored second program, the microcomputer is adapted to transfer data for rewriting the contents of the first program in the electrically erasable and programmable nonvolatile memory from the host to the electrically erasable and programmable nonvolatile memory via the interface circuit.

22. (Previously Presented) A disk drive according to claim 21,

wherein the electrically erasable and programmable nonvolatile memory further stores a fourth program which is executed by the microcomputer in response to the result of the check by using the stored second program,

wherein using the stored fourth program, the microcomputer is adapted to detect whether or not a specific command is provided to the interface circuit from the host, the specific command enables a rewrite operation of the contents of the first program in the electrically erasable and programmable nonvolatile memory, and

wherein the stored third program is executed by the microcomputer in response to the detection of the specific command.

23. (Previously Presented) A disk drive according to claim 22,

wherein the electrically erasable and programmable nonvolatile memory includes a first area in which data related to the first program is stored, and

wherein the second program includes a fifth program and a sixth program, the microcomputer obtains data related to the first program stored in the electrically erasable and programmable nonvolatile memory by executing the fifth program, and the microcomputer checks a relationship between the obtained data and the stored data in the first area by executing the sixth program.

24. (Previously Presented) A disk drive according to claim 23, wherein the microcomputer is adapted to execute the stored fourth program if the checking operation by executing the sixth program indicates that the relationship between the obtained data and the stored data in the first area is different from a predetermined relationship, and the

microcomputer is adapted to execute the stored first program if the checking operation by executing the sixth program indicates that the relationship between the obtained data and the stored data in the first area satisfies the predetermined relationship.

25. (Previously Presented) A disk drive according to claim 24, wherein the related data stored in the first area is a sum, and wherein the fifth program includes a program for obtaining a sum from the first program stored in the electrically erasable and programmable nonvolatile memory.

26. (Previously Presented) A disk drive according to claim 25, wherein the interface circuit is an ATAPI.

27. (Previously Presented) A disk drive according to claim 26, wherein the disk is an optical disk.

28. (Previously Presented) A disk drive according to claim 27, further comprising a buffer memory in which the data for rewriting the contents of the first program in the electrically erasable and programmable nonvolatile memory is stored.

29. (Previously Presented) A disk drive according to claim 28, wherein the electrically erasable and programmable nonvolatile memory is a flash memory.

30. (Currently Amended) A disk drive for reading information from a disk and outputting the read information which is to be provided to a host, comprising:

an accessing circuit which accesses the disk and generates the read information from the disk;

an interface circuit which transfers the generated read information from the accessing circuit to the host; and

a microcomputer, coupled with the accessing circuit and with the interface circuit, being formed on a semiconductor substrate and including a central processing unit and an electrically erasable and programmable nonvolatile memory,

wherein the electrically erasable and programmable nonvolatile memory stores a first program, a second program and a third program,

wherein using the stored first program, the microcomputer controls the accessing circuit so that the

operation of the accessing circuit is controlled by the stored first program,

wherein using the stored second program, the microcomputer checks data in the electrically erasable and programmable nonvolatile memory, and

wherein using the stored third program, in response to the result of the check by using the stored second program, the microcomputer transfers data for rewriting the contents of the first program in the electrically erasable and programmable nonvolatile memory from the host to the electrically erasable and programmable nonvolatile memory via the interface circuit.

31. (Previously Presented) A disk drive according to claim 30,

wherein the electrically erasable and programmable nonvolatile memory further stores a fourth program which is executed by the microcomputer in response to the result of the check by using the stored second program,

wherein using the stored fourth program, the microcomputer detects whether or not a specific command is provided to the interface circuit from the host, the specific command enables a rewrite operation of the contents of the

first program in the electrically erasable and programmable nonvolatile memory, and

wherein the stored third program is executed by the microcomputer in response to the detection of the specific command.

32. (Previously Presented) A disk drive according to claim 31,

wherein the electrically erasable and programmable nonvolatile memory includes a first area in which data related to the first program is stored, and

wherein the second program includes a fifth program and a sixth program, the microcomputer obtains data related to the first program stored in the electrically erasable and programmable nonvolatile memory by executing the fifth program, and the microcomputer checks a relationship between the obtained data and the stored data in the first area by executing the sixth program.

33. (Previously Presented) A disk drive according to claim 32, wherein the microcomputer executes the stored fourth program if the checking operation by executing the sixth program indicates that the relationship between the obtained

data and the stored data in the first area is different from a predetermined relationship, and the microcomputer executes the stored first program if the checking operation by executing the sixth program indicates that the relationship between the obtained data and the stored data in the first area satisfies the predetermined relationship.

34. (Previously Presented) A disk drive according to claim 33, wherein the related data stored in the first area is a sum, and wherein the fifth program includes a program for obtaining a sum from the first program stored in the electrically erasable and programmable nonvolatile memory.

35. (Previously Presented) A disk drive according to claim 34, wherein the interface circuit is an ATAPI.

36. (Previously Presented) A disk drive according to claim 35, wherein the disk is an optical disk.

37. (Previously Presented) A disk drive according to claim 36, further comprising a buffer memory in which the data for rewriting the contents of the first program in the

electrically erasable and programmable nonvolatile memory is stored.

38. (Previously Presented) A disk drive according to claim 37, wherein the electrically erasable and programmable nonvolatile memory is a flash memory.

39. (Currently Amended) A disk drive for reading information from a disk and outputting the read information which is to be provided to a host, comprising:

an accessing circuit which accesses the disk and generates the read information from the disk;

an ATA packet interface circuit which transfers the generated read information from the accessing circuit to the host; and

a microcomputer, coupled with the accessing circuit and with the ATA packet interface circuit, being located on a semiconductor substrate and including a central processing unit and an electrically erasable and programmable nonvolatile memory,

wherein the electrically erasable and programmable nonvolatile memory stores a first program and a second program,

wherein using the stored first program, the microcomputer controls the accessing circuit so that the operation of the accessing circuit is controlled by the stored first program,

wherein the microcomputer is adapted to judge whether or not an information according to data stored in a part of the electrically erasable and programmable nonvolatile memory satisfies a predetermined information,

wherein if the information according to data stored in the part of the electrically erasable and programmable nonvolatile memory satisfies the predetermined information, the microcomputer is adapted to detect whether or not a specific command is provided to the ATA packet interface circuit from the host, and the specific command enables a rewrite operation of the contents of the first program in the electrically erasable and programmable nonvolatile memory by the microcomputer,

wherein using the second program, in response to the detection of the specific command, the microcomputer is adapted to transfer data for rewriting the contents of the first program in the electrically erasable and programmable nonvolatile memory from the host to the electrically erasable

and programmable nonvolatile memory via the ATA packet information circuit, and

wherein if the information according to data stored in the part of the electrically erasable and programmable nonvolatile memory satisfies the predetermined information, the microcomputer executes an~~and~~ operation in accordance with the first program.

40. (Previously Presented) A disk drive according to claim 39, wherein the electrically erasable and programmable nonvolatile memory stores a third program, and wherein by using the stored third program, the microcomputer is adapted to detect whether or not the specific command is provided to the ATA packet interface circuit from the host.

41. (Previously Presented) A disk drive according to claim 40, wherein the information according to data stored in the part of the electrically erasable and programmable nonvolatile memory is a sum value of data stored in the part of the electrically erasable and programmable nonvolatile memory, wherein the predetermined information is a sum value stored in a sum value storage area included in the electrically erasable and programmable nonvolatile memory, and

wherein the satisfaction condition is that the sum value of data stored in the part of the electrically erasable and programmable nonvolatile memory is different from the sum value stored in the sum value storage area.

42. (Currently Amended) A disk drive unit, comprising:

an accessing circuit which accesses a disk, reads information from the disk and processes the read information;

an interface circuit which transfers the processed information ~~from~~ in accordance with said read information processed by the accessing circuit to a host; and

a microcomputer, coupled with the accessing circuit and with the interface circuit, ~~and~~ including a central processing unit, a first port coupled to the interface circuit, a second port, and an electrically erasable and programmable nonvolatile memory,

wherein the central processing unit, the first port, the second port, and the electrically erasable and programmable nonvolatile memory are formed on a semiconductor substrate,

wherein the electrically erasable and programmable nonvolatile memory has a write-inhibited area and a write-

enabled area ~~adapted to store therein data received from the interface circuit via the first port~~,

wherein said write-inhibited area is not enabled to write data received from the interface circuit via the first port,

wherein said write-enabled area is enabled to write data received from the interface circuit via the first port,

wherein a first program is in the write-enabled area, and a second program and a third program are in the write-inhibited area,

wherein in response to ~~an~~ a first operation ~~operating~~ of the central processing unit by executing the first program, the microcomputer is adapted to control the accessing circuit,

wherein in response to ~~an~~ a second operation ~~operating~~ of the central processing unit by executing the second program, the microcomputer is adapted to detect whether a command provided to the interface circuit from the host is a specific command or not, ~~the specific command enables~~ to enable a write operation ~~of the contents of the first program~~ for writing data to the write-enabled area in the electrically erasable and programmable nonvolatile memory ~~by the~~

~~microcomputer~~ when detecting the command being the specific command,

wherein in response to ~~an~~ a third operation ~~operating~~ of the central processing unit by executing the third program and in response to detecting the specific command, the microcomputer is adapted to transfer data, which is for ~~writing the contents of the first program~~ being written to the write-enabled area, from the ~~host~~ interface circuit via the first port to the electrically erasable and programmable nonvolatile memory via the interface circuit, and

wherein the write-inhibited area is ~~writable~~ enabled to write data received from the second port.

43. (Previously Presented) A disk drive unit according to claim 42, further comprising a serial port,

wherein the serial port is coupled to the second port.

44. (Currently Amended) A disk drive unit according to claim 42,

wherein the central processing unit further includes a serial communication interface circuit, and

wherein the second port is electrically coupled to the serial communication interface circuit ~~in~~ when a write operation ~~in~~ for writing data to the write-inhibited area is performed.

45. (Currently Amended) A disk drive unit according to claim 42,

wherein the microcomputer ~~controls loading a program for writing in~~ is adapted to transfer data, which is for being written to the write-inhibited area ~~via~~, from the second port, ~~and includes a fourth program for controlling a write operation of the program~~ to the electrically erasable and programmable nonvolatile memory, in response to a fourth operation of the central processing unit by executing a fourth program.

46. (Previously Presented) A disk drive unit according to claim 45,

wherein the central processing unit includes a boot ROM, and

wherein the fourth program is stored in the boot ROM.

47. (Currently Amended) A disk drive unit according to claim 42, further comprising a buffer memory,

wherein the data ~~to be written in~~ for writing to the write-enabled area is transferred to the buffer memory from the host via the interface circuit, and

wherein the data ~~thus~~ stored in the buffer memory is thereafter transferred to the electrically erasable and programmable nonvolatile memory.

48. (Currently Amended) A disk drive unit according to claim 45,

wherein in response to a fifth ~~program is stored in the write-inhibit area, and~~

~~wherein the central processing unit rewrites at least part of the first program to the write-enabled area by an operating of the central processing unit by executing the fifth program~~ operation of the central processing unit by executing a fifth program, the microcomputer is capable of writing data to the write-enabled area.

49. (Previously Presented) A disk drive unit according to claim 48,

wherein the electrically erasable and programmable nonvolatile memory is a flash memory.

50. (Currently Amended) A disk drive unit according to claim 42,

wherein the disk is any arbitrary one of CD-ROM, DVD, DVD-ROM, DVD-RAM, CDI, DVI, or MOD.

51. (Currently Amended) A disk drive unit according to claim 42,

wherein the interface circuit is adapted to ~~include~~ correspond to an ATAPI interface specification.

52. (New) A disk drive unit comprising:

an access control circuit;

an interface circuit; and

a microcomputer,

wherein said access control circuit controls access to a disk which is for storing information,

wherein said interface circuit controls coupling between said access control circuit and a host coupled to outside of said disk drive unit,

wherein said microcomputer is structured on a semiconductor substrate and comprises a nonvolatile memory, a central processing unit, a first port and a second port,

wherein said interface circuit controls transfer of first information which is processed from data read from said disk by said access control circuit,

wherein said nonvolatile memory includes a write permission area and a write prohibition area,

wherein said write permission area is enabled to write data received from said interface circuit via said first port and comprises an access control program executed by said central processing unit for controlling to said access control circuit,

wherein said write prohibition area is not enabled to write data received from said interface circuit via said first port and comprises an ATAPI interrupt processing program and an input control program,

wherein said central processing unit executes said ATAPI interrupt processing program for detecting whether a command, which is provided from said host to said interface circuit, is a first command or not, and when detecting that said command, which is provided from said host, is said first command by executing said ATAPI interrupt processing program,

executes said input control program for receiving first program data, which is provided from said host to said interface circuit, to be written to said write permission area, and

wherein second program data to be written to said write prohibition area is capable of being written to be received from said second port.

53. (New) A disk drive unit according to claim 52, further comprising a serial port,

wherein said serial port is coupled to said second port.

54. (New) A disk drive unit according to claim 53,

wherein said central processing unit further comprises a serial communication interface circuit, and

wherein said serial communication interface circuit is coupled to said second port, when receiving said second program data to be written to said write prohibition area.

55. (New) A disk drive unit according to claim 54,

wherein said central processing unit further comprises a boot program, and

wherein said central processing unit controls receiving of said second program data to be written to said write prohibition area, and writing of said second program data to said write prohibition area, by executing said boot program.

56. (New) A disk drive unit according to claim 55, wherein said central processing unit further comprises a read only memory for storing said boot program.

57. (New) A disk drive unit according to claim 56, further comprising a buffer memory,

wherein said first program data is received by said interface circuit from said host, is stored to said buffer memory, and is transferred from said buffer memory to said nonvolatile memory.

58. (New) A disk drive unit according to claim 57, wherein said write prohibition area further comprises a write control program, and

wherein said central processing unit controls writing of said first program data to said write permission

area as said access control program, by executing said write control program.

59. (New) A disk drive unit according to claim 58, wherein said nonvolatile memory is a flash memory.

60. (New) A disk drive unit according to claim 59, wherein said disk is any arbitrary one of CD-ROM, DVD, DVD-ROM, DVD-RAM, CDI, DVI, and MOD.

61. (New) A disk drive unit according to claim 60, wherein said interface circuit is constructed in accordance with an ATAPI interface standard.